AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-25 (Cancelled)

26. (Currently Amended) A semiconductor apparatus comprising:

a nonvolatile memory; and

a central processing unit;~~,~~

wherein said nonvolatile memory has a plurality of memory cells;~~,~~

wherein each ~~of~~ said memory ~~cells includes~~cell is a multi-bit memory cell including:

a memory gate formed over a first semiconductor region with a first insulating film and a second insulating film interposed therebetween, a plurality of data bits being stored in the memory cell by trapping electrons at one or more of a plurality of selectable portions of said second insulating film beneath said memory gate;

a first switch gate formed over said first semiconductor region to a first side of said memory gate with a third insulating film;

_____a second switch gate formed over the first semiconductor region to a second side of said memory gate with a fourth insulating film, wherein said second side is opposite said first side across said memory gate; and

_____a second semiconductor region and a third semiconductor region respectively formed adjacent to opposite sides of said first semiconductor region; and

wherein said first nonvolatile memory is capable of storing a program and data; and

wherein said central processing unit executes said program read from said first nonvolatile memory.

27. (Original) A semiconductor apparatus according to claim 26, further comprising a random access memory,

wherein said random access memory is used for a work memory for said central processing unit.

28. (Original) A semiconductor apparatus according to claim 27,

wherein said central processing unit controls to access to said nonvolatile memory.

29. (Original) A semiconductor apparatus according to claim 28, wherein said nonvolatile memory is capable of rewriting data stored therein.

30. (Original) A semiconductor apparatus according to claim 29, further comprising a second nonvolatile memory,

wherein said central processing unit controls to access to said second nonvolatile memory.

31. (Original) A semiconductor apparatus according to claim 29, further comprising a communication circuit and an antenna,

wherein said communication circuit couples to said antenna, and

wherein said communication circuit is capable of communication by electromagnetic induction.

32. (Original) A semiconductor apparatus according to claim 26,

wherein each said memory cell is capable of storing data by trapping electrons in said memory gate thereof to change a threshold voltage.

33. (New) A semiconductor apparatus comprising:

a nonvolatile memory, which is capable of storing a program and data; and

a central processing unit, which executes said program read from said nonvolatile memory,

wherein said nonvolatile memory has a plurality of memory cells,

wherein each said memory cell is a multi-bit memory cell including:

a memory gate formed over a first semiconductor region with a first insulating film and a second insulating film interposed therebetween;

a first switch gate formed over said first semiconductor region with a third insulating film and by a first side of said memory gate;

a second switch gate formed over said first semiconductor region with a fourth insulating film and by a second side of said memory gate, wherein said second side is opposite said first side across said memory gate,

a second semiconductor region and a third semiconductor region respectively formed adjacent to opposite sides of said first semiconductor region; and

wherein in a first programming operation, an electron is supplied from said third semiconductor region, moves through said first semiconductor region under said first switch gate, and is injected into a first area of said second insulating film near said first switch gate, and

wherein in a second programming operation, an electron is supplied from said second semiconductor region, moves through said first semiconductor region under said second switch gate, and is injected into a second area of said second insulating film near said second switch gate.

34. (New) A semiconductor apparatus according to claim 33, further comprising a random access memory,

wherein said random access memory is used for a work memory for said central processing unit.

35. (New) A semiconductor apparatus according to claim 34,

wherein said central processing unit controls to access to said nonvolatile memory.

36. (New) A semiconductor apparatus according to claim 35, wherein said nonvolatile memory is capable of rewriting data stored therein.

37. (New) A semiconductor apparatus according to claim 36, further comprising a second nonvolatile memory,

wherein said central processing unit controls to access to said second nonvolatile memory.

38. (New) A semiconductor apparatus according to claim 36, further comprising a communication circuit and an antenna,

wherein said communication circuit couples to said antenna, and

wherein said communication circuit is capable of communication by electromagnetic induction.

39. (New) A semiconductor apparatus according to claim 33,

wherein each said memory cell is capable of storing data by trapping electrons in said second insulating film thereof to change a threshold voltage.

40. (New) A semiconductor apparatus according to claim 33,

wherein said central processing unit is adapted to control access to said nonvolatile memory.